CLAIMS

What is claimed:

1. An electronic assembly, comprising:

a circuit board;

a package substrate, having first and second sides, attached to the circuit board;

a plurality of contact formations on the first side of the package substrate interconnecting the circuit board and the package substrate;

a stress relief layer on the first side of the package substrate, a space being defined between the stress relief layer and the circuit board; and

a microelectronic die, having an integrated circuit formed therein, mounted on the second side of the package substrate.

2. The electronic assembly of claim 1, wherein each contact formation has a height and the stress relief layer has a thickness, the thickness of the stress relief layer being less than the height of the contact formations.

3. The electronic assembly of claim 1, wherein the stress relief layer is adjacent to a portion of the contact formations that corresponds to only a portion of the height of the contact formations.

4. The electronic assembly of claim 3, wherein the heights of the contact formations are between 0.2 and 1.5 mm.

5. The electronic assembly of claim 4, wherein the stress relief layer is polymeric.

6. The electronic assembly of claim 5, wherein the stress relief layer is an adhesive paste.

7. The electronic assembly of claim 6, wherein the thickness of the stress relief layer is between 0.15 and 0.225 mm.

8. The electronic assembly of claim 7, wherein the space is an air space.

9. The electronic assembly of claim 8, wherein the microelectronic die is a microprocessor.

10. An electronic assembly, comprising:

a package substrate having first and second sides;

a microelectronic die mounted to the first side of the package substrate;

a plurality of contact formations attached to the second side of the package substrate, each having a height; and

a stress relief layer on the second side of the package substrate, the layer having a thickness less than the height of the contact formations and being adjacent to only a portion of the height of the contact formations.

11. The electronic assembly of claim 10, wherein the microelectronic die is a microprocessor.

12. The electronic assembly of claim 11, wherein the contact formations are BGA solder balls.

13. The electronic assembly of claim 12, wherein the stress relief layer is polymeric.

14. An electronic assembly, comprising:

a circuit board;

a package substrate, having first and second sides, attached to the circuit board;

a plurality of contact formations on the first side of the package substrate interconnecting the circuit board and the package substrate;

a stress relief layer between the package substrate and the circuit board; and

a microprocessor mounted on the second side of the package substrate.

15. The electronic assembly of claim 14, wherein the circuit board is a motherboard.

16. The electronic assembly of claim 15, wherein the stress relief layer is adjacent to the contact formations.

17. A method of constructing an electronic assembly, comprising:

depositing a stress relief layer on a side of a package substrate, the side having a plurality of contacts formations thereon; and

attaching the contact formations to a circuit board, a space being defined between the stress relief layer and the circuit board.

18. The method of claim 17, wherein a microelectronic die is mounted on an opposing side of the package substrate.

19. The method of claim 18, wherein the contacts have a height and the stress relief layer has a thickness, the thickness of the stress relief layer being less than the height of the contact formations.

20. The method of claim 19, wherein the stress relief layer is adjacent to a portion of the contact formations that corresponds to only a portion of the height of the contact formations.

21. The method of claim 20, wherein the stress relief layer is polymeric.

22. The method of claim 21, wherein the stress relief layer is only deposited onto selected portions of the side of the package substrate.

23. The method of claim 21, wherein the stress relief layer flows onto the package substrate.

24. The method of claim 23, wherein the stress relief layer is first deposited onto a central portion of the side of the package substrate.

25. The method of claim 21, wherein the stress relief layer is extruded onto the side of the side of the package substrate.

26. The method of claim 21, wherein the stress relief layer is a cast film, having a plurality of holes therein, and said depositing is placing the cast film on the side of the package substrate so that the contact formations extend through the holes.

27. A method comprising:

placing a plurality of semiconductor packages on a support, the semiconductor packages each having a package substrate with a first side having a microelectronic die mounted thereon and a second side with a

plurality of contact formations connected thereto, the contact formations having a height;

suspending a stencil over the semiconductor packages, the stencil having a plurality of holes; and

flowing a paste through the holes of the stencil to form a stress relief layer on the second side of the package substrate of each semiconductor package, the stress relief layer having a thickness, the thickness being less than the height of the contact formations.

28. The method of claim 27, further comprising placing the semiconductor packages onto circuit boards, the contact formations interconnecting the package substrates and the circuit board, a space being defined between the circuit board and the second side of the package substrate.

29. The method of claim 28, wherein the stress relief layer is adjacent to a portion of the contact formations that corresponds to only a portion of the height of the contact formations.

30. The method of claim 29, wherein the second sides of the package substrates face the stencil.